This work package is dedicated to explorative studies towards the development of new normally-off (E-mode) AlGaN/GaN high electron mobility transistors (HEMTs) on Si substrate. Several strategies and designs are tested and evaluated by the partners in this work package, like the use of gate oxides (MOSHEMTs) and cap layers (doped and undoped GaN). Therefore, it is important to master the processing of the devices with respect to all involved materials and fabrication steps:

- Selective etching of GaN on AlGaN (cap recess)
- Rapid thermal annealing (RTA) of the Ohmic contacts with regard to free AlGaN surface
- Deposition of gate oxides by atomic layer deposition (ALD) and characterization of the dielectric oxide layers
- Passivation of the devices

Furthermore, first characterizations of new devices are performed within the scope of this work package. This contains both DC and pulsed measurements of the HEMTs. Following reliability studies will be performed in WP7.

M12 update:

- Processes established for:
    - Selective etching of a 3 nm GaN cap on AlGaN
    - Fabrication of Ohmic contacts
    - Application of a SiN passivation layer
- Approaches towards normally-off HEMTs successfully tested
    - Polarization-engineered heterostructures, using an undoped GaN layer below the gate
        - High on/off ratio and high breakdown voltage
    - Recessed gate approach with effectively passivated thin AlGaN barriers and gate oxide
        - Several types of ALD oxides tested. Parameter variations: deposition temperatures, pre- and posttreatments (annealings, wet chemical treatments)
        - Oxide stacks analyzed
        - Low gate leakage current of 10^{-8} A/mm

M24 update:

Regarding the approach through recessing the gate, normally-off AlGaN/GaN HEMTs on Si substrates with Schottky- and MOS gates were successfully fabricated, using in situ SiN as a passivation layer. The achieved threshold voltage is +1 V. Using MOS gates, the gate leakage current could be substantially reduced ($<10^{-9}$ A/mm). In order to increase the maximum drain current, the advantageous properties of a material with larger band gap and higher polarization are desired. The development in material growth, achieved within this project (WP5 and 6), allows for the use of AlN as a barrier. Additionally, using a binary compound, hence reducing alloy scattering effects, the mobility is enhanced. Another advantage of AlN is the favorable combination with ALD oxides, due to the stability of its native oxide. First normally-off devices with AlN barrier, GaN cap and in situ SiN passivation are successfully produced and under optimization.

Within the development of polarization engineered heterostructures the high stability and polarization of AlN, in combination with a thin AlGaN layer, is used. The partial thermal or plasma oxidation of AlN in the gate area leads to normally-off operation. Devices with both thermal and plasma oxidized AlN were successfully fabricated. The threshold voltage can be adjusted by combining plasma oxidation with the scaling of low temperature ALD oxide below the gate.

In the development of high-k gate dielectrics, high stability for both ZrO_2 and Al_2O_3 is achieved. Analyses, e.g. C-V and DLTS measurements, helped in understanding the properties of the oxide/barrier interface. Low threshold voltage instability and low interface trap density is reached, applying several different treatments before and after deposition by ALD.