**WP7 – Characterization and Reliability (T0+24):**

The main goal of WP7 is to provide feedback information to the processing work packages (WP3-GaN device development and processing and WP8- Explorative technologies) in order to allow the optimization of the fabrication process at each level. This Goal will be reached through the following steps:

- Set-up a new measurements system to test the devices in real switching operation
- Carry out a full electrical and thermal characterization of the developed devices
- Experimental analysis of self-heating effects and breakdown phenomena
- Identify technological aspects for further device improvement
- Provide understanding of critical device operation conditions
- Dynamic thermal and electric field mapping using optical techniques
- Detection of potential reliability issues in an early stage of the project
- Get a sound understanding of potential degradation mechanisms
- Trigger corrective actions in processing and design iterations
- Statistical lifetime data for system life time evaluations and predictions

In the second year, mainly normally off devices, processed by WP4 (see WP4 description for more details on devices processed), have been characterized; DC, pulsed, breakdown and dynamic thermal and E-field mapping have been carried out. Traps in device active area have been identified thanks to a detailed drain current transient characterization carried out at different T. Reliability testing and failure modes and mechanisms identification activity has been started and preliminary results are very promising for the reaching of the project target.

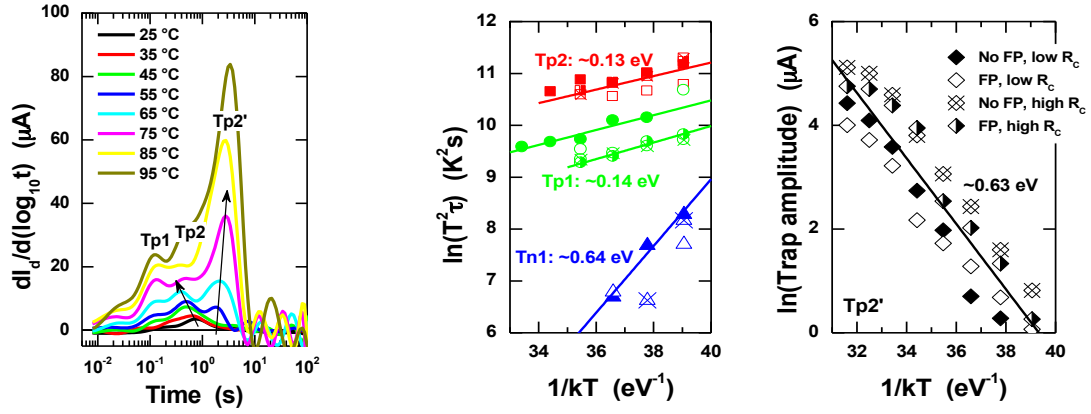
**Task 7.1 Device characterisation and analyses (T0 to T0+30)**

DC and pulsed characterization of on-wafer devices

a) DC Characterization: Devices with Carbon doped substrates (GaN:C) have high leakage current, while devices with Iron doped substrates (GaN:F) show better performances than double heterostructures AlGaN/GaN/AlGaN (GaN:AlGaN, DH): higher $I_{DS}$ and lower $R_{ON}$. $Ar^+$-implantation seems to have little effect on DC parameters in Ga:Fe wafer. AlGaN/GaN/AlGaN devices have different behaviors whether they have $Ar^+$ implantation or not: implanted devices have lower $I_{DS}$ and higher $V_{Th}$.
b) Pulsed characterization: In pulsed measurements, $Ar^+$-implantation on SiC cause a threshold voltage shift in both AlGaN/GaN/AlGaN and GaN:Fe wafer; this suggests increased traps population into the buffer layer under the gate. In C-doped devices, $g_m$ peak reduction and $R_{ON}$ increase are also observed.
c) Vertical leakage measurements and substrate biasing effects: $I_D$-$V_G$ measurements reveal an increased leakage in off-state when the SiC substrate is grounded; the effect is more pronounced (approximately one order of magnitude) on Fe-doped GaN than the DH. In both cases the $Ar^+$-implantation effectively suppress the substrate current.

**Study of parasitic effects (traps) and characterization of devices at different temperatures**

*Trapping analysis of normally-ON SB-HEMTs (GBT08-14).* Trap levels were determined from the Arrhenius plot of $t_e$ as a function of inverse temperature (T) (Fig. 1a and 1b). Strong increase in de-trapping effects with positive transient was observed with increased T, with a new peak labeled as Tp2' dominating the transient completely for T>70 °C. The activation energy ($E_a$) of this new peak was ~0.63 eV (Fig. 1 c). Similar $E_a$ of Tp1 and Tp2 (~0.14 eV) is consistent with the hopping effect limiting the two-step de-trapping process. In contrast, Tn1 shows $E_a$ of 0.64 eV that may be related to the bulk level in GaN.




a) b) c)

Fig. 1 a) $I_d$-transient analyses measured at different $T_b$ for HEMTs with high $R_C$ without FP. b) Arrhenius plots for trap level extraction with and without FP for both $R_C$ values based on the $t_e$-$T_b$ dependence and c) based on a new dominant peak amplitude rise with $T_b$. Measurement conditions: $V_{gs,F}$=-10 V, $V_{ds,F}$=0.5 V, $t_F$=1 s, $V_{gs,M}$=1 V, $V_{ds,M}$=0.5 V.

**Rdson characterization**

The static Rdson as a function of the Vgs @ Ids=5A measured on packaged devices showing a Rdson value between 92 and 102 mOhm, that correspond to RdsonxA=1Ωmm$^2$, a value which is comparable to the best-in-class superjunction Si-MOSFET (CoolMOS C7 by Infineon), but not better, as it would be needed. For that reason a new optimized layout has been already released with expected devices in 12/2013.

Rdson-transient performed on wafer level. Double heterostructure devices with C buffer compensation (DH:C) samples show a much lower initial dynamic Rdson collapse if compared with Single heterostructure devices with C buffer compensation (SH:C), suggesting that the introduction the AlGaN back-barrier is beneficial for the suppression of the dynamic Rdson collapse. A further improvement is obtained through the use of double heterostructure devices without any carbon doping (DH). An almost complete suppression of the Rdson collapse was obtained by using the single-heterostructure devices with iron-buffer compensation (SH:Fe). The results of the current transients for the SH:C, DH:C, and DH samples, reveal the presence of three distinct traps: H1 (detected only in the SH:C devices), E1 and E2 (detected in the SH:C, DH:C and DH devices), which are thermally-activated.

- H1, has been identified as a deep-acceptor state with activation energies and cross sections of 0.84eV/3x10$^{-13}$cm$^2$. H1 could be introduced by the Carbon-doping.
- E1 and E2 (detected in the SH:C, DH:C and DH samples), with activation energies and cross sections of 0.85eV/4x10$^{-14}$cm$^2$, and 0.83eV/1x10$^{-15}$cm$^2$ respectively.

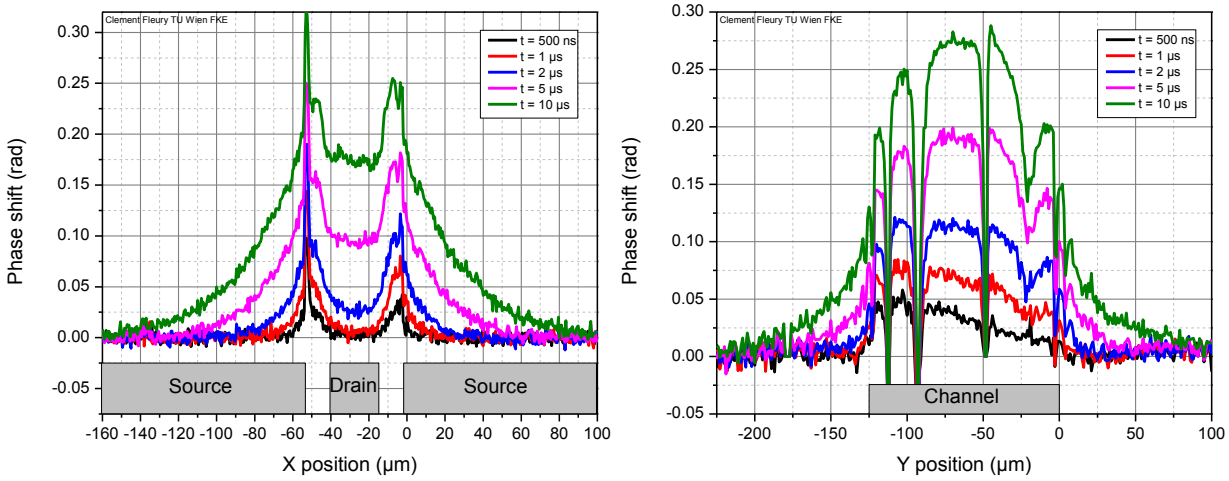
**Investigation of breakdown mechanisms from DC and transient IV measurements**

These devices show 600V capability with an off-state drain current of 7µA/mm. Analysis of vertical leakage current and vertical breakdown (VB) in HEMT test structures of FBH fabricated on Si (GBT08-14, EpiGan substrate) and SiC substrates (GPG02-09,13 and GPG15,16,17,18) has been carried out. Samples with different substrate doping, heterostructure design (AlGaN, C or Fe-doped buffer), with and without Ar-implant in the SiC substrate have been analysed. Temperature dependent measurements have shown the existence of two components of vertical leakage current with a stronger (around 0.3eV) and a weaker thermal activation. VB measurements have been performed aimed to the VB path localization. A methodology based on DC IV measurement in the current-controlled mode and pulsed stress excitation using a transmission line pulser has been developed for device biasing. VB path have been analysed from the back side using infrared microscopy and from top side. The failure analysis confirmed the filamentary nature of VB damage, with better damage space resolution in the case of the pulsed stressing. The role of material defects and of self-heating effect (using thermal simulation in conjunction with WP3) on VB has been evaluated. Time evolution of vertical leakage current has also been studied, revealing a time dependent breakdown behaviour, at least in the high voltage (>470V) range.

## Task 7.2 Dynamic thermal and E-field mapping (T0+6 to T0+30)

TUW continues in thermal analysis of normally-off p-GaN gate devices of FBH. Devices of older (GPG02-09, GPG02-13, carbon doped buffer) and newer technology runs were analysed (GPG15-AlGaN buffer, GPG17-Fe-doped buffer, non Ar-implanted). The thermal distribution in the devices have been analysed as a function of drain bias under a constant gate bias, and under a constant dissipated power. Hot spots, their position movement with drain bias, and the current homogeneity along the gate width have been studied, see Fig. 4. Our analysis shows that the devices biased above 150V can sometimes undergo a cumulative

damage which is characterized by decreased reflectivity properties and increase in the off-state current. This damage, occurring during short-circuited load operation, should however not represent a reliability risk for normal operation. Thermo-optical simulation (in conjunction with WP3) has also been performed to support the experimental data. The simulation can reproduce the data in a limited temperature range, showing a need of more refined physical model. As well the preliminary analysis of optical artefacts indicates a need of deeper simulation study.

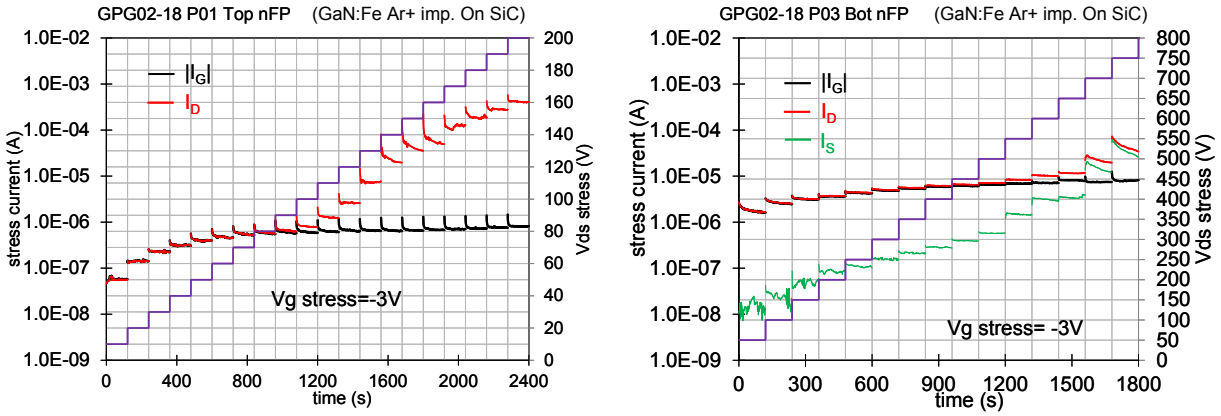



**(a)** **(b)**

Fig. 4 TIM scanning across (a) and along (b) the gate width of a double finger test HEMT (GPG 15). Sharp phase minima in (b) are due to optical artefacts related to low reflectivity areas.3.2.2.4

## Task 7.3 Identification of degradation mechanisms (T0+6 to T0+36)

Off-state step-stresses with substrate floating show very high breakdown voltages (up to 800V) and progressive degradation of electrical properties during tests (Fig. 5). When the substrate is grounded no degradation is observed, but the breakdown voltage drastically reduces to less than 200V, due to parasitic path between the top and the bottom layer that causes vertical leakage and eventually yields to catastrophic degradation.



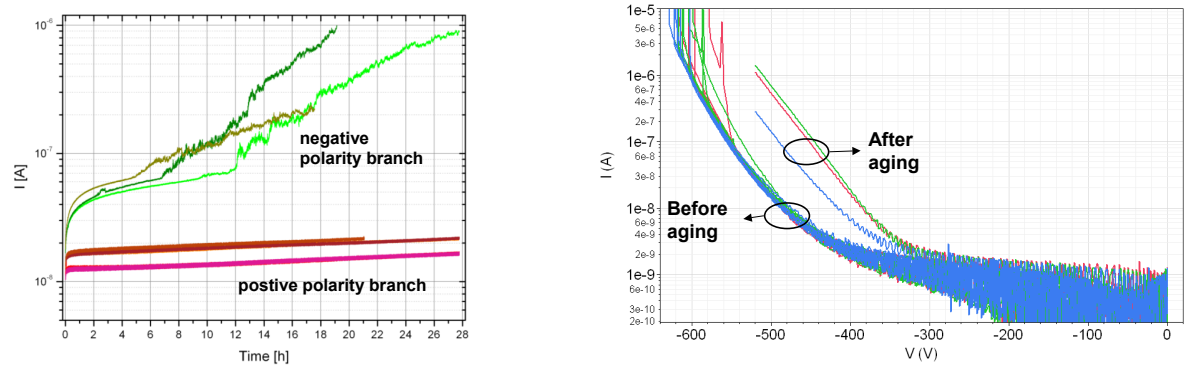

**(a)** **(b)**

**Figure 5: Off-state step-stress with substrate (a) grounded and (b) floating.**

## Task 7.4 Reliability testing and systematic lifetime characterization (T0+12 to T0+36)

DC lifetime tests performed on vertical test structures have shown that the vertical leakage current gradually increases with time, see Fig. 6 a) and b). The test devices have been stressed in the negative and the positive branch of the vertical I/V characteristics at voltages of 500 V and 300 V respectively. This selection of voltage levels ensures identical leakage current values at the beginning of the tests. As the vertical IV-characteristics is asymmetric in positive and negative branch, different voltage levels are required to force the same vertical leakage current. Only a very weak dependency of the leakage current has been observed during stressing in the positive branch, however stressing in the negative branch results in quite a fast increase of the leakage within the first few minutes followed by a slower steady increase. After a number of stress hours a strong fluctuation of vertical leakage starts with a tendency to increase gradually as bias

stressing continues. As shown in Fig. 1 b) this increase of vertical leakage is non-reversible - a degradation of the buffer structure has occurred.




a) b)

Fig. 6: Vertical high voltage tests performed on 3 test devices for positive and negative polarity at room temperature: The tests have been performed at 500 V and 300 V for the positive and the negative branch respectively to ensure same leakage current values at the beginning of the tests. a) Time dependency in positive and negative b) Vertical leakage IV characteristics of the complete device ensemble (before aging) and of 3 devices subjected to vertical DC-storage tests (after aging)

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